AMENDMENT

In the claims:

This listing of claims will replace all prior versions and listings of claims in the application.

1. (Cancelled)

2. (Currently Amended) A method comprising:

analyzing input terms on a bit-wise basis to segment each level of bit significance of input terms into one or more groups of three bits, and/or one or more groups two bits and/or one or more groups of one bit;

selecting resources to generate a summing module based, at least in part, on the analysis; and

designing a hyperpipelined series of Boolean function generators to implement a Wallace-architecture of full-adders to receive at least a portion of the one or more groups of three bits, half-adders to receive at least a portion of the one or more the groups of two bits, and associated registers to receive at least a portion of the one or more the groups of one bit in the selected resources, the series of Boolean function generators to combine the input terms to produce intermediate summation results.

3. (Cancelled)

4. (Previously Presented) The method of claim 2 wherein selecting resources to generate the summing module comprises selecting atomic elements of a dedicated logic device in which to implement the Wallace-architecture of full-adders, half-adders, and associated registers.

5. (Previously Presented) The method of claim 4 wherein selecting atomic elements of a dedicated logic device in which to implement the Wallace-architecture comprises selecting atomic elements of a field programmable gate array (FPGA) in which to implement the Wallace-architecture of full-adders, half-adders, and associated registers.

6. (Previously Presented) The method of claim 4 wherein selecting atomic elements of a dedicated logic device in which to implement the Wallace-architecture comprises control logic in a device with a block of dedicated logic selecting atomic elements of the dedicated logic in which to implement the Wallace-architecture of full-adders, half-adders, and associated registers.

7. (Previously Presented) The method of claim 4 wherein selecting resources to generate the summing module based, at least in part, on the analysis further comprises:

determining a minimal number of full-adders, half-adders, and associated registers with which the Wallace-architecture could be implemented; and

selecting atomic elements of the dedicated logic device so as to reduce a number of atomic elements left unused in the design, to implement the Wallace architecture with a number of full-adders, half-adders, and associated registers that approaches the minimum number.

8. (Previously Presented) The method of claim 4 wherein selecting resources to generate the summing module based, at least in part, on the analysis further comprises:

selecting atomic elements of the dedicated logic device to implement the Wallace-architecture of full-adders, half-adders, and associated registers; and

wherein designing the hyperpipelined series of Boolean function generators comprises assigning proximate atomic elements functions so as to reduce routing distances between stages of the Wallace-architecture.

9. (Previously Presented) The method of claim 4 wherein selecting resources to generate the summing module based, at least in part, on the analysis further comprises:

determining a minimal number of full-adders, half-adders, and associated registers with which the Wallace-architecture could be implemented; and

wherein designing the hyperpipelined series of Boolean function generators comprises selecting atomic elements of the dedicated logic device to implement the Wallace-architecture with the minimal

number of full-adders, half-adders, and associated registers while concurrently assigning proximate atomic elements to functions that result in reducing routing distances between stages of the Wallace-architecture.

10. (Previously Presented) The method of claim 2 wherein selecting resources to generate the summing module comprises a system controller selecting one or more field programmable gate arrays (FPGAs) in the system in which to implement the Wallace-architecture of full-adders, half-adders, and associated registers, and wherein designing the hyperpipelined series of Boolean function generators to implement the Wallace-architecture of full-adders, half-adders, and associated registers in the selected resources comprises the system controller designing the hyperpipelined series of Boolean function generators to be implemented with the atomic elements of the selected FPGA(s).

11. (Previously Presented) The method of claim 2 wherein designing the hyperpipelined series of Boolean function generators to implement the Wallace-architecture comprises designing the hyperpipelined series of Boolean function generators to increase grouping of bits of a same level of bit-significance of the input terms.

12. (Previously Presented) The method of claim 2 wherein designing the hyperpipelined series of Boolean function generators comprises dynamically designing the hyperpipelined series of Boolean function generators to implement desired instances of the Wallace-architecture.

13. (Previously Presented) The method of claim 2 further comprising:

implementing the design in the dedicated logic device by assigning the atomic elements of the dedicated logic device according to the design.

14. (Previously Presented) The method of claim 2 further comprising:

utilizing the summing module with other components of a processing system;

identifying features of the other components that can be integrated into the design of the Wallace-architecture; and

wherein designing the hyperpipelined series of Boolean function generators includes integrating the identified features into the Wallace-architecture.

15. (Previously Presented) The method of claim 14 wherein designing the hyperpipelined series of Boolean function generators includes adding accumulator bits from the other components to a summation result achieved by the Wallace-architecture.

16. (Previously Presented) The method of claim 14 wherein designing the hyperpipelined series of Boolean function generators includes coupling the Wallace-architecture to output a summation result to at least one of the other components.

17. (Currently Amended) An article of manufacture comprising a machine-accessible medium having content to provide instructions for generating a complex arithmetic summing module, the content to provide the instructions to cause an electronic system to:

analyze input terms on a bit-wise basis to segment each level of bit significance of input terms into one or more groups of three bits, and/or one or more groups two bits and/or one or more groups of one bit;

select resources to generate a summing module based, at least in part, on the analysis; and

design a hyperpipelined series of Boolean function generators to implement a Wallace-architecture of full-adders to receive at least a portion of the one or more groups of three bits, half-adders to receive at least a portion of the one or more the groups of two bits, and associated registers to receive at least a portion of the one or more the groups of one bit in the selected resources, the series of Boolean function generators to combine the input terms to produce intermediate summation results.

18. (Cancelled)

19. (Previously Presented) The article of manufacture of claim 17 wherein the content to provide instructions to cause the electronic system to select resources to generate the summing module comprises the content to provide instructions to cause the electronic system to select atomic elements of a dedicated logic device in which to implement the Wallace-architecture of full-adders, half-adders, and associated registers.

20. (Previously Presented) The article of manufacture of claim 19 wherein the content to provide instructions to cause the electronic system to select atomic elements of a dedicated logic device in which to implement the Wallace-architecture comprises the content to provide instructions to cause the electronic system to select atomic elements of a field programmable gate array (FPGA) in which to implement the Wallace-architecture of full-adders, half-adders, and associated registers.

21. (Previously Presented) The article of manufacture of claim 19 wherein the content to provide instructions to cause the electronic system to select atomic elements of a dedicated logic device in which to implement the Wallace-architecture comprises the content to provide instructions to cause the electronic system to direct control logic in a device with a dedicated logic array to select atomic elements of the dedicated logic in which to implement the Wallace-architecture of full-adders, half-adders, and associated registers.

22. (Previously Presented) The article of manufacture of claim 19 wherein the content to provide instructions to cause the electronic system to select resources to generate the summing module based, at least in part, on the analysis further comprises the content to provide instructions to cause the electronic system to:

determine a minimal number of full-adders, half-adders, and associated registers with which the Wallace-architecture could be implemented; and

select atomic elements of the dedicated logic device so as to reduce a number of atomic elements left unused in the design, to implement the Wallace architecture with a number of full-adders, half-adders, and associated registers that approaches the minimum number.

23. (Previously Presented) The article of manufacture of claim 19 wherein the content to provide instructions to cause the electronic system to select resources to generate the summing module based, at least in part, on the analysis further comprises the content to provide instructions to cause the electronic system to:

select atomic elements of the dedicated logic device to implement the Wallace-architecture of full-adders, half-adders, and associated registers; and

wherein the content to provide instructions to cause the electronic system to design the hyperpipelined series of Boolean function generators comprises the content to provide instructions to cause the electronic system to assign proximate atomic elements functions so as to reduce routing distances between stages of the Wallace-architecture.

24. (Previously Presented) The article of manufacture of claim 19 wherein the content to provide instructions to cause the electronic system to select resources to generate the summing module based, at least in part, on the analysis further comprises the content to provide instructions to cause the electronic system to:

determine a minimal number of full-adders, half-adders, and associated registers with which the Wallace-architecture could be implemented;

wherein the content to provide instructions to cause the electronic system to design the hyperpipelined series of Boolean function generators comprises the content to provide instructions to cause the electronic system to select atomic elements of the dedicated logic device to implement the Wallace-architecture with the minimal number of full-adders, half-adders, and associated registers and concurrently to assign proximate atomic elements to functions to result in reducing routing distances between stages of the Wallace-architecture.

25. (Previously Presented) The article of manufacture of claim 17 wherein the content to provide instructions to cause the electronic system to select resources to generate the summing module comprises the content to provide instructions to cause the electronic system to direct a controller to select one or more field programmable gate arrays (FPGAs) coupled with the controller in which to implement the Wallace-architecture of full-adders, half-adders, and associated registers, and wherein the content to provide instructions to cause the electronic system to design the hyperpipelined series of Boolean function generators to implement the Wallace-architecture of full-adders, half-adders, and associated registers in the selected resources comprises content to provide instructions to cause the electronic system to direct the controller to design the hyperpipelined series of Boolean function generators to be implemented with the atomic elements of the selected FPGA(s).

26. (Previously Presented) The article of manufacture of claim 17 wherein the content to provide instructions to cause the electronic system to design the hyperpipelined series of Boolean function generators to implement the Wallace-architecture comprises the content to provide instructions to cause the electronic system to design the hyperpipelined series of Boolean function generators to increase grouping of bits of a same level of bit-significance of the input terms.

27. (Previously Presented) The article of manufacture of claim 17 wherein the content to provide instructions to cause the electronic system to design the hyperpipelined series of Boolean function generators comprises the content to provide instructions to cause the electronic system to dynamically design the hyperpipelined series of Boolean function generators to implement desired instances of the Wallace-architecture.

28. (Previously Presented) The article of manufacture of claim 17 further comprising the content to provide instructions to cause the electronic system to:

implement the design in the dedicated logic device by assigning the atomic elements of the dedicated logic device according to the design.

29. (Previously Presented) The article of manufacture of claim 17 further comprising the content to provide instructions to cause the electronic system to:

utilize the summing module with other components of a processing system;

identify features of the other components that can be integrated into the design of the Wallace-architecture; and

wherein the content to provide instructions to cause the electronic system to design the hyperpipelined series of Boolean function generators includes the content to provide instructions to cause the electronic system to integrate the identified features into the Wallace-architecture.

30. (Previously Presented) The article of manufacture of claim 29 wherein the content to provide instructions to cause the electronic system to design the hyperpipelined series of Boolean function generators includes the content to provide instructions to cause the electronic system to add accumulator bits from the other components to a summation result achieved by the Wallace-architecture.

31. (Previously Presented) The article of manufacture of claim 29 wherein the content to provide instructions to cause the electronic system to design the hyperpipelined series of Boolean function generators includes the content to provide instructions to cause the electronic system to couple the Wallace-architecture to output a summation result to at least one of the other components.